

Appl. No. 10/657,132
Amendment dated: December 26, 2006
Reply to OA of: July 25, 2006

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1 (currently amended). A thermal enhance semiconductor package, comprising:
a carrier having an upper surface and a lower surface opposed to the upper surface;

a semiconductor chip having an active surface[[,]] and a back surface opposed to the active surface [[and]], wherein the semiconductor chip further comprises a plurality of bonding pads formed on the active surface;

a plurality of conductive devices, ~~which are formed on~~ connecting the bonding pads ~~and connect the active surface of the semiconductor~~ and the upper surface of the carrier; and

a universal heat spreader disposed on the back surface of the semiconductor chip and having an outer surface and an inner surface, wherein the inner surface of the universal heat spreader faces the back surface of the semiconductor chip, and the universal heat spreader further comprising:

a plurality of through holes, ~~the universal heat spreader disposed on the back surface of the semiconductor chip, wherein~~ passing through the outer surface and the inner surface of the universal heat spreader; and

a plurality of heat transmission pins [[are]] disposed in one part of the through holes[[,]];

wherein air convection is provided via the other part of the through holes, and the heat is transferred from the inside of the thermal enhance semiconductor package to the outside of the thermal enhance semiconductor package.

Claims 2 and 3(canceled).

4(currently amended). The thermal enhance semiconductor package of claim

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1, ~~wherein~~ further comprising a copper layer formed on an outer surface of the heat transmission pin ~~has an outer surface and a copper layer is formed on the outer surface.~~

5(currently amended). The thermal enhance semiconductor package of claim 4, wherein a material of the universal heat spreader comprises copper or aluminum.

Claim 6(canceled).

7(currently amended). The thermal enhance semiconductor package of claim ~~[[6]] 5, wherein one of the through holes has an inner wall and a cooper layer is formed on the inner wall~~ further comprising a copper layer formed on an inner wall of the through holes.

8(currently amended). The thermal enhance semiconductor package of claim 1, ~~wherein~~ further comprising a silver layer formed on an outer surface of the heat transmission pin ~~has an outer surface and a silver layer is formed on the outer surface.~~

9(currently amended). The thermal enhance semiconductor package of claim 8, wherein a material of the universal heat spreader comprises copper or aluminum.

Claim 10(canceled).

11(currently amended). The thermal enhance semiconductor package of claim ~~[[10]] 9, wherein one of the through holes has an inner wall and a copper layer is formed on the inner wall~~ further comprising a copper layer formed on an inner wall of the through holes.

12(currently amended). The thermal enhance semiconductor package of claim

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1, further comprising a heat transmission adhesive formed between the back surface of the semiconductor chip and ~~[[a]]~~ the inner surface of the universal heat spreader.

13(previously presented). The thermal enhance semiconductor package of claim 1, further comprising a stiffener ring connecting the carrier and the universal heat spreader via a heat transmission adhesive.

14(original). The thermal enhance semiconductor package of claim 13, wherein the stiffener ring is disposed surrounding the semiconductor chip.

15(currently amended). The thermal enhance semiconductor package of claim 1, further comprising ~~a filler~~ an underfill disposed between the upper surface of the carrier and the active surface of the semiconductor chip.

16(original). The thermal enhance semiconductor package of claim 1, wherein one of the conductive devices is a conductive bump.

17(original). The thermal enhance semiconductor package of claim 1, wherein a plurality of solder balls are formed on the lower surface of the carrier.

Claim 18-23(canceled).

24(new). A thermal enhance semiconductor package, comprising:
a carrier having an upper surface and a lower surface opposed to the upper surface;
a semiconductor chip having an active surface and a back surface opposed to the active surface, wherein the semiconductor chip further comprises a plurality of bonding pads formed on the active surface;
a plurality of conductive devices, connecting the bonding pads and the upper

surface of the carrier; and

a universal heat spreader disposed on the back surface of the semiconductor chip and having an outer surface and an inner surface, wherein the inner surface of the universal heat spreader faces the back surface of the semiconductor chip, and the universal heat spreader further comprising:

a plurality of through holes passing through the outer surface and the inner surface of the universal heat spreader; and

a plurality of heat transmission pins disposed in one part of the through holes to increase the area for heat dissipation, wherein the disposing location of the heat transmission pins is adjustable to achieve the designed thermal resistance;

wherein air convection is provided via the other part of the through holes, and the heat is transferred from the inside of the thermal enhance semiconductor package to the outside of the thermal enhance semiconductor package.

25(new). The thermal enhance semiconductor package of claim 24, wherein the heat transmission pin has an outer surface and a copper layer is formed on the outer surface.

26(new). The thermal enhance semiconductor package of claim 24, further comprising a heat transmission adhesive formed between the back surface of the semiconductor chip and a surface of the universal heat spreader.

27(new). The thermal enhance semiconductor package of claim 24, further comprising a stiffener ring connecting the carrier and the universal heat spreader via a heat transmission adhesive.

28(new). The thermal enhance semiconductor package of claim 24, further comprising an underfill disposed between the upper surface of the carrier and the active surface of the semiconductor chip.

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29(new). The thermal enhance semiconductor package of claim 24, wherein one of the conductive device is a conductive bump.

30(new). The thermal enhance semiconductor package of claim 24, wherein a plurality of solder balls are formed on the lower surface of the carrier.